

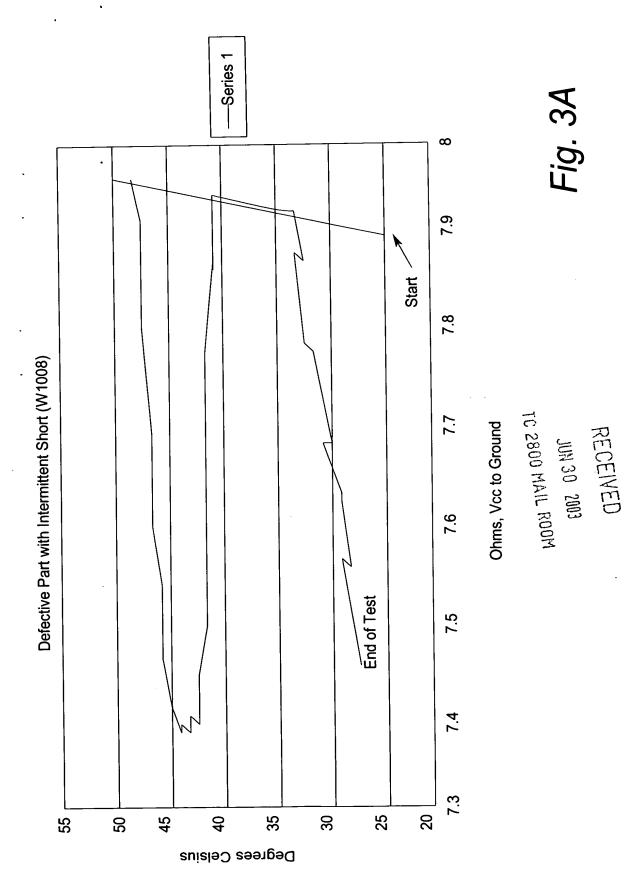
Fig. 2A

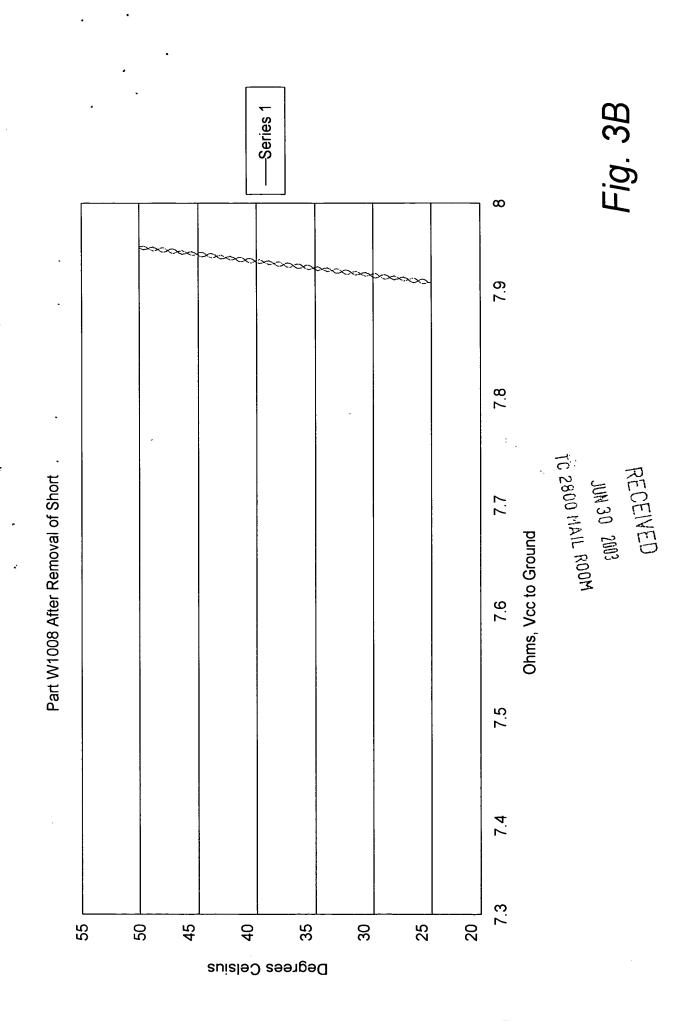


Multichip Ceramic Package 28 48 44 46 IC IC IC 40 VCC Power Bus 29b 49x 29x 39x 49b 29a 39a 39b 49a 29c R 39c 49c 29x 39x 49x Ground 42 R= measured resistance during temperature ramp-up and ramp-down

Fig. 2B









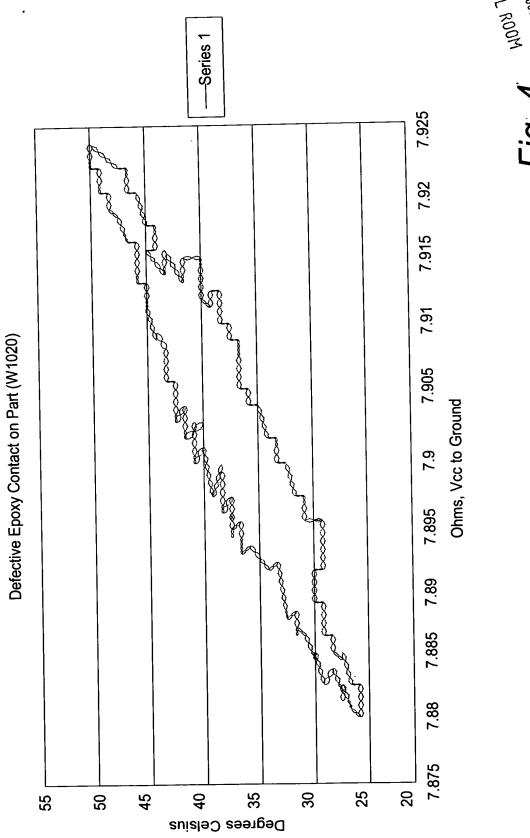
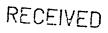


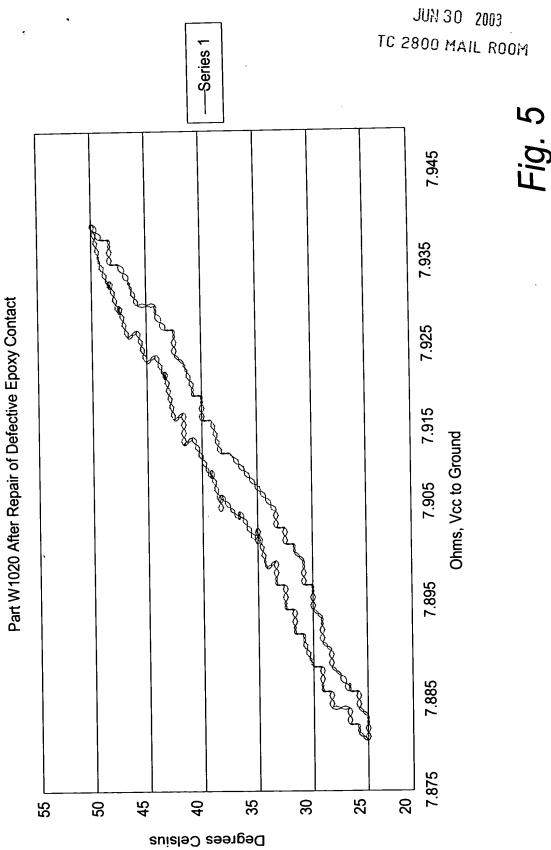
Fig. 4

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TC 2800 MAIL ROOM







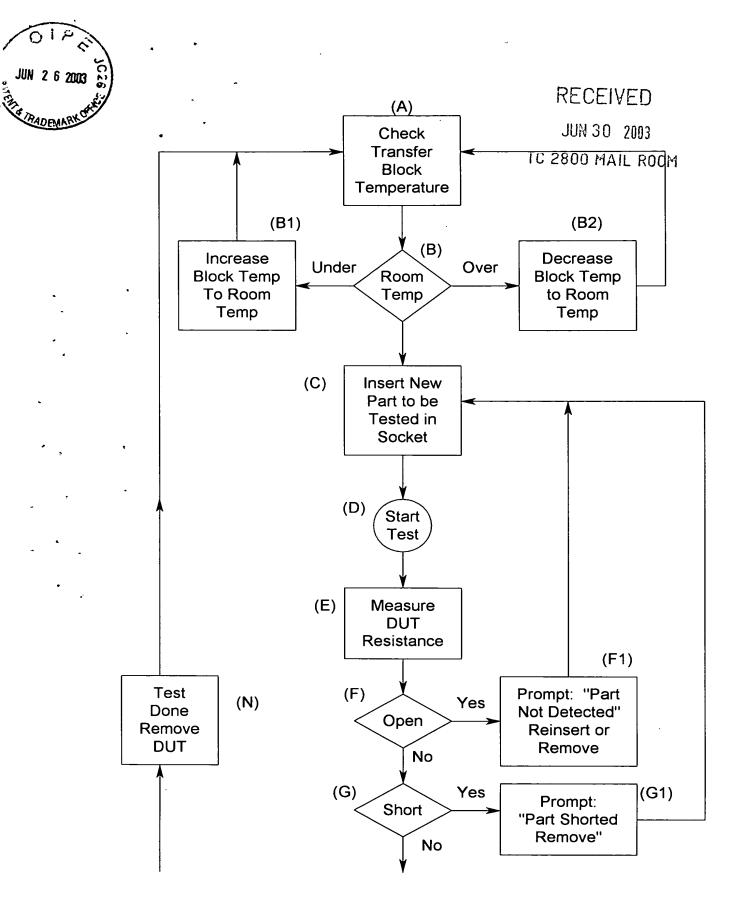


Fig. 6A

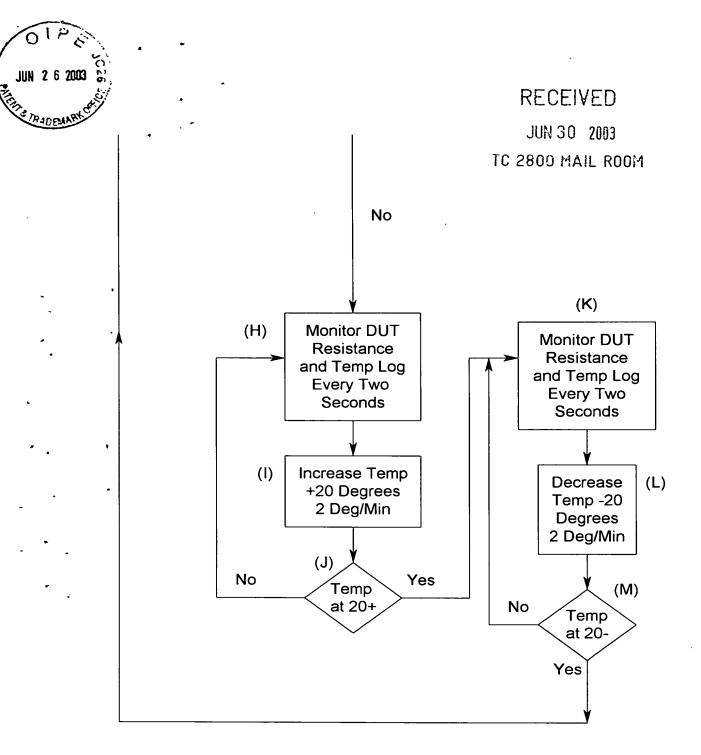


Fig. 6B